REMARKS

Reconsideration of the above-referenced application in view of the following remarks is respectfully requested.

Claims 1, 2, and 4-22 were pending in this application. Claim 22 has been cancelled.

The Examiner acknowledged receiving the proposed drawing modifications in the last response, but asserted that there was no written reference nor a request for approval for the drawings in the response. These comments are not understood by Applicant in view of the fact that Applicant's last response contained the following statements on page 3:

> . . . a proposed modification to the drawings is included herewith to show that the die, leads, and interposer pads are supported on a substrate in both prior art Figures 1 and 3, as well as in the embodiments of the invention shown in Figures 2, 4, 5, and 6. Support for the drawing modifications can be found on page 2 of the specification in the "Summary of Invention" section, where the interposer pads are described as being "on an electro-less substrate between the semiconductor die and the lead."

These statements clearly constitute the "written reference" to the drawings. As far as the request for approval, Applicant's reference to the drawings as including a "proposed modification" make clear Applicant's intent to have the modification approved for entry. The Examiner's allegation that the drawing modifications constitute new matter is addressed in the statements quoted above as well as elsewhere in this response.

Claims 1, 2, and 4-22 stand rejected under 35 U.S.C. 112, first paragraph. The point of contention in this rejection is whether the original disclosure supports the attached features recited whereby a first end of a wire is attached by a ball bond and second end by a stitch bond and the first end of a second wire is attached by a ball and the second end by a stitch bond. The Examiner asserts that the only stitch feature is discussed on page 4, line 8 with regard to the bond on lead 26. The Examiner further argues that Figure 4 fails to show the recited stitch features. Applicant respectfully replies as follows: Figure 2 shows one wire (20) attached with a ball bond 12 to die 10. Figure 2 also shows a wire (24) attached with a ball bond 23 to pad 21 and by stitch bond 25 to lead 26. Wire 20 is clearly also attached to pad 21. Since only one ball 23 appears on pad 21, it follows that wire 20 is attached by a stitch bond. One skilled in the art would appreciate that fact in view of the relatively flat profile of a stitch bond that facilitates bonding thereon with a subsequent ball bond. Therefore, Applicant respectfully requests that the rejection be withdrawn.

Claim 22 has been cancelled thereby obviating the rejection of that claim.

Claims 1, 2, and 4-21 stand rejected under 35 U.S.C. 112, first paragraph. Specifically, the Examiner asserts that the structure of the interposer substrate is unclear. Applicant submits that the existence of a substrate is clearly implied in the drawings. The proposed modifications to the drawings show that the die, leads, and interposer pads are supported on a substrate in both prior art Figures 1 and 3, as well as in the embodiments of the invention shown in Figures 2, 4, 5, and 6. Support for the drawing modifications can be found on page 2 of the specification in the "Summary of Invention" section, where the interposer pads are described as being "on an electro-less substrate between the semiconductor die and the lead." Applicant respectfully requests approval and entry of these drawing modifications. Regarding the term "electroless", Applicant submits that the term taken literally means "insulating." Thus, the die, leads, and interposer pads are formed on an insulating substrate, which is known in the art.

The Examiner also asserts that the specification does not support the term "ball grid array." However, the skilled artisan will appreciate that Figures 5 and 6 are top views of an insulating substrate, the underside of which includes pads coupled to leads 15 and 25 in Figure 5 and to leads 65 and 15 in Figure 6. Figures 1 to 4 have been modified accordingly. It is known in the art to form solder balls on such pads. As stated in the specification, leads 15, 25, and 65 are only representative of the many such leads formed on the substrate. Hence, the underside of the substrate includes many such corresponding pads to which solder balls may be attached; hence, the term "ball grid array." The Examiner's statement on page 5 of the Office Action that "[p]ads connected to leads are further not conventionally bound to a solder bond substrate underside arrangement" is not understood by Applicant. As indicated in the instant specification, the Microstar ball grid array package from Texas Instruments Incorporated is a package in which leads and pads are connected to solder balls as shown in Figures 1-4. Thus, the Examiner's statement that such an arrangement is not conventional is not understood by Applicant.

In view of the electroless or insulating nature of the substrate, the interposer pad is "electrically floating" by virtue of being located on the insulating substrate, a fact which would be appreciated by the skilled artisan.

Claim 3 has been cancelled thereby obviating the rejection of that claim.

Regarding the "plurality of interposer pads", Figure 6 shows two interposer pads 21 and 63 which form a plurality.

Regarding the Applicant's alleged failure to show an "electroless substrate" and a "ball grid array", the proposed drawing modifications included in the last response address this. The fact that such things may have a variety of structural appearances is not relevant as long as the modifications to the drawings are supported in the specification. As Applicant has indicated above, the proposed drawing modifications are supported in the specification when that specification is read in view of the skilled artisan's understanding of the art.

Claims 1-22 stand rejected under 35 U.S.C. 102(e) as being anticipated by Schmidt, et al. Claims 3 and 22 have been cancelled. Claim 1 includes the steps of "attaching a first end of a first bonding wire to a semiconductor die with a ball bond; attaching a second end of the first bonding wire to an interposer pad with a stitch bond; attaching a first end of a second bonding wire to the interposer pad with a ball bond; and attaching the second end of the second bonding wire to the lead with a stitch bond." Schmidt teaches away from the claimed invention by forming only ball bonds ("welds" in Schmidt's terminology) on his leads 3 and only stitch (or "wedge") bonds on connection surfaces 4. In col. 4, lines 30-37, Schmidt states that this is done to save space on leads 3. In view of this teaching away, Applicant respectfully submits that Claim 1, as amended, as well as Claims 2 and 4-7 which depend therefrom, are patentable over Schmidt.

Claim 8 includes the feature of "a plurality of bonding wires attached to the semiconductor die with ball bonds and to the leads with stitch bonds, said wires attached to said interposer pads." As indicated above, Schmidt does not disclose such a feature. In fact, Schmidt teaches away from forming stitch bonds on leads. Therefore, Applicant submits that Claim 8 and Claims 9-15 which depend therefrom are patentable over Schmidt.

Claim 16 includes the steps of "coupling the die to the plurality of interposer pads with a first plurality of bonding wires ball bonded to said die and stitch bonded to said interposer pads; and coupling the plurality of interposer pads to the plurality of leads with a second plurality of bonding wires ball bonded to said interposer pads and stitch bonded to said leads." As indicated above, Schmidt does not teach or suggest such steps. Therefore, Applicant submits that Claim 16, as well as Claims 17-21 which depend therefrom, are patentable over Schmidt.

In view of the above, Applicant respectfully requests the entry of this amendment, the withdrawal of the Examiner's rejections, and allowance of

Claims 1, 2, and 4-21. If the Examiner has any questions or other correspondence regarding this application, Applicant requests that the Examiner contact Applicant's attorney at the below listed telephone number and address.

Respectfully submitted,

Texas Instruments Incorporated
P.O. Box 655474, M/S 3999
Dallas, TX 75265
Phone: 972 917-5653
Fax: 972 917-4418

Michael K. Skrehot
Reg. No. 36,682